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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/682,128 | 10/07/2003 | Sung-Ho Kim | 4591-347 | 1351 |

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| EXAMINER | |
|---|---|
| MAI, ANH D | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2814 | |

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/682,128 | KIM, SUNG-HO | |
| | Examiner | Art Unit | |
| | Anh D. Mai | 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *8-13 and 20-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 14-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/7/2003; 9/20/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

1. Claims 8-13 and 20-23 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on March 22, 2005.

### *Specification*

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested:

NONVOLATILE MEMORY DEVICE HAVING ASYMMETRIC SOURCE/DRAIN REGION.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 14-17 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al. (U.S. Patent No. 6,429,472).

With respect to claim 14, Kim teaches a nonvolatile memory device as claimed including:

first (14) and second (16) impurity regions on a substrate (12) separated by a first channel region and a second channel region, the first channel region being wider than the second channel region and the first impurity region (14) being wider than the second (16) impurity region.

With respect to claim 15, the device of Kim further includes a tunnel insulating layer (60), a charge storing layer (62), and a gate interlayer insulating layer (64/65) disposed on the substrate (12) in the first channel region.

With respect to claim 16, the gate interlayer insulating layer (64) extends over the substrate (12) in the second channel region.

With respect to claim 17, the device of Kim further comprises a control gate (69) disposed over the first and second regions.

With respect to claim 19, the device of Kim further comprises:

a control gate (69) crossing over the first channel region and the second channel region; and

a tunnel insulating layer (60), a charge storing layer (62), and a gate interlayer insulating layer (64/65) interposed between the control gate (69) and the substrate (12) in the first channel region, wherein the gate interlayer insulating layer (64/65) is interposed between the control gate (69) and the substrate (12) in the second channel region.

*Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Kim '472.

With respect to claim 14, AAPA teaches a split gate-type SONOS device substantially as claimed including:

a substrate (2);

a first impurity region (16d) and a second impurity region (16s) formed in the substrate (12), separated by a first channel region ($L_1$) and a second channel region ($L_2$);

a control gate (12) crossing over the first channel region ($L_1$) and the second channel region ($L_2$); and

a tunnel insulating layer (6), a charge storing layer (8), and a gate interlayer insulating layer (10) interposed between the control gate (12) and the substrate (2) in the first channel region ($L_1$), wherein the gate interlayer insulating layer (10) is interposed between the control gate (12) and the substrate (2) in the second channel region ($L_2$).

Thus, AAPA is shown to teach all the features of the claim with the exception of forming the split gate-type memory device such that the first channel region and the first impurity region are wider than the second channel region and the second impurity region, respectively.

However, Kim teaches a split gate-type memory device including the first channel region and the first impurity region (14) are wider than the second channel region and the second impurity region (16), respectively. (See Figs. 5A-C and 6F).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the first channel region and the first impurity region of AAPA wider than the second channel region and the second impurity region as taught by Kim to improve the program/erase efficiency and the endurance characteristic.

With respect to claim 2, the first impurity region (16d) of AAPA is a drain region and the second impurity region (16s) is source region.

With respect to claim 3, the sides of the tunnel insulating layer (6), the charge storing layer (8), and the gate interlayer insulating layer (10 of AAPA) are aligned with the side of the control gate (12).

With respect to claim 4, the control gate (12) of AAPA is formed of polycrystalline silicon.

With respect to claim 5, the charge storing layer (8) of AAPA is formed of silicon nitride.

With respect to claim 6, the tunnel insulating layer (6) of AAPA is formed of silicon oxide.

With respect to claim 7, the gate interlayer insulating layer (10) is formed of silicon oxide.

5. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim '472 as applied to claim 17 above, and further in view of AAPA.

Kim teaches a nonvolatile memory device as described in claim 14 above including: the control gate (69) is formed of polycrystalline silicon, the charge storing layer (62) is formed on the tunnel insulating layer (60) of silicon oxide.

Thus, Kim is shown to teach all the features of the claim with the exception of using silicon nitride for the charge storing layer.

However, AAPA teaches other material such as silicon nitride are well known to be used for charge storing layer.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the charge storing layer of Kim utilizing silicon nitride as taught by AAPA to reduce the programming and erase operation voltage. This is well known in the art.

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 9:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH D. MAI
PRIMARY EXAMINER
March 29, 2005